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| APPLICATION NO.           | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---------------------------|-------------|----------------------|---------------------|------------------|
| 09/648,095                | 08/25/2000  | Akella V.S. Satya    | KLA1P016F           | 4627             |
| 22434                     | 7590        | 02/22/2005           | EXAMINER            |                  |
| BEYER WEAVER & THOMAS LLP |             |                      | VU, QUANG D         |                  |
| P.O. BOX 70250            |             |                      | ART UNIT            |                  |
| OAKLAND, CA 94612-0250    |             |                      | PAPER NUMBER        |                  |
|                           |             |                      | 2811                |                  |

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/648,095

Applicant(s)

SATYA ET AL.

Examiner

Quang D. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 November 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 108-121 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 108-121 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 108, 109, 114, 115, 116 and 117 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,959,459 to Satya et al. in view of US Patent No. 6,309,956 to Chiang et al. and Japanese Patent No. 02-087544 to Munakata.

Regarding claim 108, Satya et al. (figure 1) teach a method of fabricating a semiconductor die, comprising:

forming a test structure on the semiconductor die (column 3, lines 43-45), wherein the test structure permits voltage contrast testing (column 2, lines 19-23); and

performing voltage contrast testing on the test structure to detect electrical defects within the test structure (column 3, lines 32-42; column 4, line 8 – column 5, line 16).

Satya et al. differ from the claimed invention by not showing a dummy structure in a top of conductive layer. However, Chiang et al. (figure 5) teach dummy structure (597) in a top of conductive layer (520). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chiang et al. into the device taught by Satya et al. in order to improve the strength of semiconductor interlayers,

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improves mechanical reliability and minimizes dishing between interconnects of semiconductor devices.

The combined device differs from the claimed invention by not showing a dummy structure uses in the test structure. However, Munakata teaches the dummy testing (abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Munakata into the device taught by Satya et al. and Chiang et al. in order to evaluate the quality and reliability of the wiring on the semiconductor device.

Regarding claim 109, the combined device shows a substrate (Chiang et al.; 500); and at least one contact (Chiang et al.; 590), which couples the dummy structure (Chiang et al.; 597) to the substrate (Chiang et al.; 500).

Regarding claim 114, the combined device shows forming a plurality of test structures on the semiconductor die, wherein at least a portion of each test structure includes a dummy structure (Chiang et al.; 597), wherein the test structures permit voltage contrast testing and wherein some of the test structures also include contacts for coupling its dummy structure (Chiang et al.; 597) to a substrate of the semiconductor die and others of the test structures remain floating; and performing voltage contrast testing on the test structures to detect electrical defects within the test structures.

Regarding claim 115, the combined device shows scanning an electron beam over the dummy structures (Chiang et al.; 597) to thereby cause electron emission from the dummy structures; and determining that a particular one of the dummy structures (Chiang et al.; 597) and

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its associated test structure has a defect between the substrate and the dummy structure by analyzing the electron emission from the dummy structures.

Regarding claim 116, the combined device shows the defect is an open defect (Satya et al.; column 4, lines 18-23).

Regarding claim 117, the combined device shows a first conductive layer portion (Chiang et al.; 520) underneath the dummy structure (Chiang et al.; 597); and a via (Chiang et al.; 590) coupling the first conductive layer portion (Chiang et al.; 520) to the dummy structure (Chiang et al.; 597).

3. Claims 110, 112, 113, 118 and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satya et al. and Chiang et al. in view of Munakata, and further in view of US Patent No. 6,001,733 to Huang et al.

The disclosures of Satya et al., Chiang et al. and Munakata are discussed as applied to claims 108-109 and 114-117 above.

Regarding claim 110, the combined device shows a first conductive layer portion (520) over the substrate (500) and underneath the dummy structure (597); a second isolation layer (555) between the first conductive layer portion (520) and the dummy structure (597); and a second contact (590) for coupling the first conductive layer portion (520) to the dummy structure (597).

The combined device differs from the claimed invention by not showing a first isolation layer between the first conductive layer portion and the substrate. However, Huang et al. (figures 3A-E) teach a first isolation layer (304) between the first conductive layer portion (330)

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and the substrate (300). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Huang et al. into the device taught by Satya et al., Chiang et al. and Munakata because it is desirable to reduce the coupling capacitance between conductive layer and substrate.

The combined device differs from the claimed invention by not showing a first contact for coupling the substrate to the first conductive layer portion. However, Huang et al. (figures 3A-E) teach a first contact (via [324]) for coupling the substrate (300) to the first conductive layer portion (330). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Huang et al. into the device taught by Satya et al., Chiang et al. and Munakata because it is desirable to provide interconnection between the substrate and the upper conductive layer.

Regarding claim 112, the combined device shows scanning an electron beam over the dummy structure (Chiang et al.; 597) to thereby cause electron emission from the dummy structure; and determining that the test structure has a defect between the substrate and the dummy structure (Chiang et al.; 597) when electron emission is impeded from the dummy structure.

Regarding claim 113, the combined device shows the defect is an open defect (Satya et al.; column 4, lines 18-23).

Regarding claim 118, the combined device shows a substrate (500) underneath the first conductive layer portion (520).

The combined device differs from the claimed invention by not showing a via coupling the first conductive layer portion to the substrate. However, Huang et al. (figures 3A-E) teach a

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first contact (via [324]) for coupling the substrate (300) to the first conductive layer portion (330). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Huang et al. into the device taught by Satya et al., Chiang et al. and Munakata because it is desirable to provide interconnection between the substrate and the upper conductive layer.

Regarding claim 120, the combined device shows the test structure comprises a plurality of stacked conductive layers and vias (Chiang et al.; 590) to form a multilevel test structure.

4. Claims 111, 119 and 121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satya et al., Chiang et al. and Munakata in view of Huang et al., and further in view of US Patent No. 3,861,023 to Bennett.

The disclosures of Satya et al., Chiang et al., Munakata and Huang et al. are discussed as applied to claims 110, 112, 113, 118 and 120 above.

Regarding claim 111, the combined device differs from the claimed invention by not showing at least one of the first and second contacts is a redundant type contact. However, Bennett teaches redundant via (column 15, lines 32-42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Bennett into the device taught by Satya et al., Chiang et al., Munakata and Huang et al. because it is desirable to reduce the parasitic capacitance between the upper layer and the lower layer.

Regarding claim 119, the combined device differs from the claimed invention by not showing the via is a redundant via. However, Bennett teaches redundant via (column 15, lines

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32-42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Bennett into the device taught by Satya et al., Chiang et al., Munakata and Huang et al. because it is desirable to reduce the parasitic capacitance between the upper layer and the lower layer.

Regarding claim 121, the combined device differs from the claimed invention by not showing the via is a redundant via. However, Bennett teaches redundant via (column 15, lines 32-42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Bennett into the device taught by Satya et al., Chiang et al., Munakata and Huang et al. because it is desirable to reduce the parasitic capacitance between the upper layer and the lower layer.

### ***Response to Arguments***

Applicant's arguments with respect to claims 108-121 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

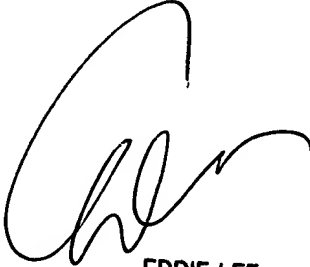
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv  
January 21, 2005



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SUPERVISORY PATENT EXAMINER  
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